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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Serial No. 09/410,646	Confirmation No.: 7191
Application of: David A. EDWARDS	Customer No.: **30429**
Filed: October 1, 1999	
Art Unit: 2113	
Examiner: M. MASKULINSKI	
Attorney Docket No. 99-TK-565-SS	
For: CIRCUIT FOR MONITORING INFORMATION ON AN INTERCONNECT	

APPELLANT'S BRIEF UNDER 37 CFR 1.192

MAIL STOP APPEAL BRIEF - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I. Real Party in Interest

STMicroelectronics Inc.
1310 Electronics Drive
Carrolton, TX 75006

II. Related Appeals and Interferences

No other appeals or interferences are currently known to Appellant that will directly affect, be directly affected by, or have a bearing on the decision to be rendered by the Board of Patent Appeals and Interferences in the present appeal.

III. <u>Status of the Claims</u>

Claims 1 and 3-26 are pending in the application. No claims have been allowed. On April 5, 2004, Appellants appealed from the final rejection by filing a Notice of Appeal of all pending claims.

IV. <u>Status of Amendments</u>

The amendments filed August 7, 2002, December 30, 2002, February 24, 2003, and July 14, 2003 have been entered.

V. <u>Summary of the Invention</u>

Briefly, the inventions of claims 1 and 16 are directed towards circuits (e.g., bus analyzer 40 in Fig. 3 and Fig. 4) for monitoring information packets (Fig. 2A and Fig. 2B) on an interconnect (22 in Fig. 1) and Fig. 3. The packets are defined, and described in Fig. 2A and Fig. 2B, as comprising a number of fields containing information including both data and packet routing information. The claimed invention involves and is inextricably entwined with packet data communication interconnections. The specification sets out detailed examples of packet formats on pages 10-11 describing Fig. 2A and Fig. 2B. The term "packet" is used throughout the specification in a manner that is consistent with the commonly understood meaning of the term.

The invention of claims 24 and 26 relates to circuits having one or more modules (14, 16, 18 and 20 in Fig. 1) connected to put information packets (Fig. 2A and Fig. 2B) on an interconnect (22 in Fig. 1) and Fig. 3. In the invention of claim 24, an arbiter 28 determines which module is permitted to put information onto the interconnect 22, which is described at page 9, line 27. The invention of claim 26 calls for circuitry (e.g., arbiter 28) for determining if the information in a packet matches one or more conditions and then prevents a module from putting further information packets onto the interconnect (e.g., as described at page 21, lines 16-23).

The invention of claim 25 describes a method involving monitoring information-containing packets on an interconnect (e.g., using bus analyzer 40), determining when the information in the packet satisfies one or more conditions

(e.g., using watch point comparator 48) and preventing a module from putting information packets onto the interconnect when the information in the packet satisfies a condition (e.g., as described at page 21, lines 16-23).

VI. <u>Issues</u>

A. <u>Whether claims 1, 3, 7-9 11-14, 16 and 18-25 are anticipated by Wolff et al.</u>

B. <u>Whether claims 1, 16, 24, 25, and 26 are anticipated by Goodrum et al.</u>

C. <u>Whether Wolff et al. alone or in combination with Cepulis, Ardini, Jr. et al., Pizzica, Bersteyn et al, and/or Merrill et al supports an obviousness rejection of claims 4-6, 10, 15, 17 and 26.</u>

VII. <u>Grouping of Claims</u>

Claims 1 and 3-26 stand or fall together.

VIII. <u>Argument</u>

A. <u>Whether claims 1, 3, 7-9, 11-14, 16 and 18-25 are anticipated by Wolff et al.</u>

The examiner has maintained that Wolff et al. show the circuit set out in claims 1, 16, 24 and 25, as well as the various specific claim elements set out in dependent claims 3, 7-9, 11-14, 18-21 and 23-25. While it is appreciated that the Examiner must take the broadest reasonable meaning for claim terminology when examining claims, it is respectfully believed that the construction of claim terminology being applied to reject the instant claims violate the accepted meanings for those terms.

In particular, claims 1, 16, 24 and 25 each call for, in varying language, <u>information packets</u>. The Wolff et al. reference shows two parallel busses, referred to at col. 3, lines 61-64 as the "A bus" and the "B bus", that function to duplicate each other. The A bus and B bus each comprise an identical set of signals. The set of signals described by Wolff et al would not be confused as a packet by anyone of skill in the art of data communication. This set of signals is

akin to a circuit-switched connection in which a circuit connection is made between communicating ends of the bus.

The "set of signals" in Wolff et al. does not show or suggest the claimed information packets. The Examiner chooses to construe the definition of a packet as "a serial stream of clocked data bits" (see, e.g., final Office action mailed 2/4/04, page 16, lines 6-8). There is no authority cited for this definition, and this definition contradicts the commonly accepted meaning of the word "packet" as set out in various authoritative definitions of record:

First, Appellant made of record a definition of a packet in a data communication network, as provided by the Modern Dictionary of Electronics, Sixth Ed., Howard W. Sams & Company, 1988, which is "a group of bits, including data and control elements that is switched and transmitted as a unit."

Second, the Examiner proffered a similar definition from IEEE 100, The Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, and states "that a packet in its broadest definition is a unit of data of some finite-size that is transmitted as a unit" (see Office action of 4/14/2003, page 13). Both the first and second definitions are consistent in that they include the concept of a unit of data that is transmitted as a unit. A "serial stream" of clocked data bits does not define a "unit of data" and so is inconsistent with, and impermissibly broader than, the Examiners own definition of "packet". Although it is recognized that a data stream can be encapsulated in packets, clearly one of skill in the art would recognize that a stream and a packet are different. Yet, this is the crux of the Office's reliance on Wolff et al. to reject claims 1 and 22.

As a third definition, Appellant made of record Newton's Telecom Dictionary, 18th Edition (2002), which describes three principle elements of a "packet" as:

1) Header—control information such as synchronizing bits, address destination or target device, address of originating device, length of packet, etc.

2) Text or payload—the data to be transmitted.

3) Trailer—end of packet and error detection and correction bits."

While it is believed that the term packet as used in the claims as originally filed was clear and definite, in the spirit of cooperation claims 1 and 22 were amended to explicitly use a more narrow definition of the word "packet" including packet routing information. Packet routing information, described generally at page 5 of the specification, is a particular type of information that does not appear in a bus-type interconnect of the Wolff reference. The set of signals in Wolff et al. is not routed—it is coupled end-to-end by the physical interconnect. The set of signals in Wolff et al. do not contain routing information as there is but one source and one destination possible. The set of signals in Wolff et al. is not a unit of data, it is a collection of separate signals. Accordingly, Wolff et al. do not show a packet as called for in claims 1 and 22.

Using yet another definition from Newton's Telecom Dictionary, an "Information Packet" is defined as:

"A bundle of data sent over a network. The protocol used determines the size and makeup of the packet."

In Wolff et al, the size of the set of information is determined by the number of signal lines (called "sets of conductors in col. 3, line 60) in the bus, and not by a protocol used. In contrast, the claims call for packets of information in the ordinary meaning of that term where the packet size is determined by a protocol choice, not a hardware limitation.

The patent office itself recognizes in the Manual of Classification (see class 370/352, for example) that packet switching is a distinct, defined type of switching that is different from circuit switched type connections as shown in the Wolff et al. reference.

Further, claims 1, 16 and 25 call for a determination of whether the information in a packet satisfies one or more conditions. Because Wolff et al. compare a binary signal to another binary signal there is one and only one

"condition" that can be satisfied. Specifically, Wolff et al. can only determine if the signals match, and determine if any other condition is satisfied.

For at least these reasons, claims 1, 16, 24 and 25 as well as claims 3, 7-9, 11-14, 16, 18-21 and 23 that depend from claims 1 and 16 are believed to be allowable over Wolff et al.

B. Whether claims 1, 16, 24, 25, and 26 are anticipated by Goodrum et al.

Like the Wolff et al. reference discussed above, Goodrum et al. do not show or suggest monitoring information from packets containing information (or information-containing packets). Goodrum et al. describe several bus types including PCI, EISA, and local bus. None of these are described as packet bus architectures or as conveying packets. It is quite telling that in 185 pages of text and drawings, Goodrum does not once use the word "packet". Nevertheless, the Office Action states that "In the Abstract, Goodrum et al disclose...an interconnect and a plurality of modules connected to said interconnect for putting packets of information onto the interconnect..." The Abstract contains no such language, and the Office action simply uses Appellant's claim as a template for abstracting the word "bus" into a rejection.

Further, the Examiner points to Goodrums' Fig. 15A and column 14 as showing packets. However, Goodrum et al. do not call these illustrations "packets". These are disclosed as phases of a transaction, or contents of a memory queue. They are not a unit of data of finite size that is transmitted as a unit. Accordingly, this element of claims 1, 16, 24, 25 and 26 is not shown or suggested in the reference.

C. Whether Wolff et al. alone or in combination with Cepulis, Ardini, Jr. et al., Pizzica, Bersteyn et al, and/or Merrill et al supports an obviousness rejection of claims 4-6, 10, 15, 17 and 26.

The Examiner has relied on a variety of other references in combination with Wolff et al. to supply various features of dependent claims 4-6, 10, 15, and 17, which all depend from claim 1, as well as independent claim 26.

Essentially, none of these references show or suggest that one would modify the conventional bus shown in Wolff et al. to use a packet bus, and then to receive packets of information, determine if parts of those packets of information satisfy one or more conditions, and then perform one or more actions based on a determination that the information in the packet satisfies one or more conditions.

It is almost remarkable, but the word "packet" does not appear even one time in Cepulis, Ardini, Jr. et al., Pizzica, Bersteyn et al, and/or Merrill et al. Accordingly, it is believed that Wolff et al. in combination with any or all of these reference cannot show or suggest the features of independent claims 1, 16, and 26. For at least these reasons, claims 4-6, 10, 15, 17 and 26 are not made obvious by the applied references.

IX. Conclusion

In view of all of the above claims 1 and 3-26 are believed to be allowable and the case in condition for allowance and it is respectfully requested that the Examiner's rejections be overturned.

Respectfully submitted,

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I. APPENDIX OF CLAIMS ON APPEAL

1. A circuit for monitoring information packets including both data and packet routing information, wherein the information packets are put onto an interconnect by one or more modules, wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data, said circuit comprising:

circuitry for determining if the information in a packet matches one or more conditions; and

circuitry for preventing a module from putting further information packets onto said interconnect if it is determined that information on the interconnect matches said one or more conditions.

2. (Cancelled).

3. A circuit as claimed in claim 1, wherein said information comprises requests and responses.

4. A circuit as claimed in claim 1, wherein said circuitry for preventing a module from putting further information onto the interconnect comprises a register.

5. A circuit as claimed in claim 4, wherein the register comprises one bit for each module and the value of said bit determines if the respective module is prevented from putting further information into the interconnect.

6. A circuit as claimed in claim 4, wherein a location is defined in said register for each module, the location being independent of the address of the module used by the interconnect.

7. A circuit as claimed in claim 1, wherein the module which puts the information onto the interconnect which matches the one or more conditions is prevented by the preventing circuitry from being granted access to the interconnect.

8. A circuit as claimed in claim 1, wherein the determining circuitry comprises comparator circuitry which compares the information on the interconnect with one or more match conditions.

9. A circuit as claimed in claim 1, wherein said conditions comprise one or more preconditions and one or more match conditions, said circuitry for preventing a module from putting information onto said interconnect when said one or more preconditions and said one or more match conditions occur.

10. A circuit as claimed in claim 9, wherein one precondition is that the one or more match conditions have occurred a predetermined number of times.

11. A circuit as claimed in claim 9, wherein one precondition is that the circuit is enabled.

12. A circuit as claimed in claim 9, wherein one precondition is that circuitry external to said circuit has been enabled.

13. A circuit as claimed in claim 12, wherein said external circuitry is a latch.

14. A circuit as claimed in claim 9, wherein said match conditions comprise one or more of the following:

an address or address range of the information;

the module or modules which put the information onto the interconnect;

the module or modules which are intended to receive the information on the interconnect; and

the type of transaction to which the information relates.

15. A circuit as claimed in any preceding claim, wherein storing circuitry is provided to store the information which satisfies the at least one condition.

16. A functional circuit comprising: an interconnect;

one or more modules connected to the interconnect; and

a monitoring circuit for monitoring information packets put onto the interconnect by one or more modules, said information packets including both data and packet routing information, wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data and said monitoring circuit comprising:

circuitry for determining if the information packet on the interconnect matches one or more conditions; and

9

circuitry for preventing a module from putting further information onto said interconnect if it is determined that information packet on the interconnect matches said one or more conditions.

17. A circuit as claimed in claim 16, wherein the circuit is an integrated circuit.

18. A circuit as claimed in claim 16, wherein an arbiter is provided for arbitrating between the modules to determine which module is granted access to the interconnect at a given time, said arbiter being connected to the preventing circuitry, the arbiter and the preventing circuitry being arranged so that a module which is prevented from putting further information onto the interconnect is prevented from winning an arbitration.

19. A circuit as claimed in claim 18, wherein said determining circuitry is at least partially in the arbiter.

20. A circuit as claimed in claim 16, wherein said interconnect is a bus.

21. A circuit as claimed in claim 16, wherein one of said modules comprises a debug module.

22. A circuit as claimed in claim 16, wherein said preventing circuit is in said debug module.

23. A circuit as claimed in claim 22, wherein at least part of the determining circuitry is in the debug module.

24. A circuit comprising:

an interconnect;

one or more modules connected to the interconnect to put information packets onto the interconnect, wherein the information packets comprise both data and packet routing information, and wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data;

an arbiter for determining which module is permitted to put information packets onto the interconnect; and

10

circuitry for preventing a module from putting further information packets onto said interconnect, said preventing circuitry preventing a module from winning an arbitration carried out by said arbiter.

25. A method comprising the steps of:

monitoring information packets on an interconnect, the information comprising data and packet routing information and being put onto the interconnect by one or modules, wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data;

determining if the information on an interconnect satisfies one or more conditions; and

preventing a module from putting information packets onto an interconnect if it is determined that the information satisfies one or more conditions.

26. A circuit for monitoring packet information put onto an interconnect by one or more modules, wherein said interconnect is not a circuit-switched bus, wherein each packet comprises a number of fields containing information, including a routing field, an address field, a source field, a transaction type field, a transaction identifier field, wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules, said circuit comprising:

circuitry for determining if the information in a packet matches one or more conditions; and

circuitry for preventing a module from putting further information packets onto said interconnect if it is determined that information on the interconnect matches said one or more conditions.